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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,084	07/31/2003	Gerard Chauvel	TI-35428 (1962-05407)	2214

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,084	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/28/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has not been filed in parent Application No. 10/632084, filed on July 29, 2003.

Oath/Declaration

Receipt is acknowledged of papers filed under 35 U.S.C. 119 (a)-(d) based on an application filed in 10/632084 on 07/29/2003. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath, declaration or application data sheet does not acknowledge the filing of any foreign application. A new oath, declaration or application data sheet is required in the body of which the present application should be identified by application number and filing date.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Objections

Claims 6, 9, and 20 are objected to because of the following informalities:

As per claim 6:

The applicant misspelled "predetermined" (line 1). Appropriate correction is required.

As per claims 9 and 20:

The applicant omits the word "from" from the phrase selected (from) the group consisting of. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Toy US Pat no. 4,314,350.

As per claim 1:

Toy teaches a processor executing a plurality of instructions (Fig 1, # 100, column 2, lines 51-54), comprising: an arithmetic logic unit (Fig 10, # 102 & 103, lines 46-60); and a plurality of registers coupled to the ALU, each register programmable to store a register value (Figures 11-14); wherein said processor executes a test and skip instruction that includes a first register reference and a second register reference (column 4, lines 18-25) and causes the processor to compare the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison (column 4, lines 27-37).

As per claim 2:

Toy teaches the processor of claim 1 wherein the second value comprises a register value stored in the second register reference (Fig 2, # 214, column 4, lines 32-36).

As per claim 3:

Toy teaches the processor of claim 1 wherein the processor is configured to access memory and the second value is stored in the memory (Fig 1, # 110, column 2, lines 49-53).

As per claim 4:

Toy teaches the processor of claim 3 wherein the second register reference contains a value used to compute a pointer to a memory location containing the second value (Fig 1 # 108, column 2, lines 52-57).

As per claim 5:

Toy teaches the processor of claim 4 wherein the pointer is computed by adding the value from the second register reference to a register value from another register (columns 5-6, lines 68-8).

As per claim 6:

Toy teaches the processor of claim 5 wherein the value held in the another register is post-incremented by a predetermined value following execution of the test and skip instruction (column 4, lines 18-22).

As per claim 7:

Toy teaches the processor of claim 1 wherein the comparison includes a condition that is specified in the test and skip instruction (Figure 1 # 104, column 3, lines 47-52).

As per claim 8:

Toy teaches the processor of claim 7 wherein any one of a plurality of conditions are specified in the test and skip instruction (Fig 2 # 203, columns 3-4, lines 65-5).

As per claim 9:

Toy teaches the processor of claim 7 wherein the condition is a condition selected the group consisting of equal to, not equal to, less than, and greater than (column 3, lines 23-31).

As per claim 10:

Toy teaches a method of executing a test and skip instruction, comprising: examining a bit in the test and skip instruction (column 3, lines 37-40), determining an address mode based on said bit (Fig 1 # 107-109, column 1, lines 52-57); comparing contents of a first register to contents of a second register if the bit is in a first state (Fig 11 # 1007, column 7, lines 17-20); or comparing the contents of the first register to contents of a non-register location if the bit is in a second state (column 3, lines 8-11), and skipping a subsequent instruction based on results of the comparison (column 4, lines 46-51).

As per claim 11:

Toy teaches the method of claim 10 wherein skipping the subsequent instruction comprises replacing the subsequent instruction with a no operation instruction (column 4, lines 19-21).

As per claim 12:

Toy teaches the method of claim 10 wherein the non-register location is a location selected from the group consisting of memory and a stack (column 3, lines 8-11).

As per claim 13:

Toy teaches a system, comprising: a main processor unit (Fig 2 # 101); and a co-processor (Fig 2 # 203) coupled to said main processor unit, wherein said co-processor executes a test and skip instruction that includes a first register reference and a second register reference (column 4, lines 18-30) and causes the processor to compare the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference (Fig 11 # 1000 & 1007) and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison (column 4, lines 46-49).

As per claim 14:

Toy teaches the system of claim 13 wherein the second value comprises a register value stored in the second register reference (Fig 2, # 214, column 4, lines 32-36).

As per claim 15:

Toy teaches the system of claim 13 wherein the processor is configured to access memory and the second value is stored in the memory (Fig 1, # 110, column 2, lines 49-53).

As per claim 16:

Toy teaches the system of claim 15 wherein the second register reference contains a value used to compute a pointer to a memory location containing the second value (Fig 1 # 108, column 2, lines 52-57).

As per claim 17:

Toy teaches the system of claim 16 wherein the pointer is computed by adding the value from the second register reference to a register value from another register (columns 5-6, lines 68-8).

As per claim 18:

Toy teaches the system of claim 13 wherein the comparison includes a condition that is specified in the test and skip instruction (Figure 1 # 104, column 3, lines 47-52).

As per claim 19:

Toy teaches the system of claim 18 wherein any one of a plurality of conditions are specified in the test and skip instruction (Fig 2 # 203, columns 3-4, lines 65-5).

As per claim 20:

Toy teaches the system of claim 18 wherein the condition is a condition selected the group consisting of equal to, not equal to, less than, and greater than (column 3, lines 23-31).

As per claim 21:

Toy teaches the system of claim 13 wherein the system comprises a communication device (column 2, lines 9-16).

As per claim 22:

Toy teaches a programmable logic device comprising; control logic (column 1, lines 51-56) and a means for executing a test and skip instruction that includes a first register reference identifying a first register having a register value and a second register reference identifying a second register also having a register value (Figures 11-14); for comparing the register value stored in the first register and a second value associated with the second register (column 3, line 50-55), and for executing or not executing a subsequent instruction that follows the test and skip instruction based on the comparison (column 4, lines 46-49).

As per claim 23:

Toy teaches the system of claim 22 wherein said second value is stored in a register (Fig 2, # 214, column 4, lines 32-36).

As per claim 24:

Toy teaches the system of claim 22 wherein said second value is stored in memory (Fig 1, # 110, column 2, lines 49-53).

As per claim 25:

Toy teaches the system of claim 22 wherein said second value is stored in a stack (column 3, lines 8-11).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10, 13, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Kreitzer US Pat no. 5,253,349 A.

As per claim 1:

Kreitzer teaches a processor executing a plurality of instructions (column 1, lines 45-46), comprising: an arithmetic logic unit (Fig 1 "ALU", lines 38-40); and a plurality of registers coupled to the ALU, each register programmable to store a register value (Figures 1 # 4, column 2, lines 13-17); wherein said processor executes a test and skip instruction that includes a first register reference and a second register reference (column 1, lines 58-60) and causes the processor to compare the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison (column 1, lines 51-58).

As per claim 10:

Kreitzer teaches a method of executing a test and skip instruction, comprising: examining a bit in the test and skip instruction (column 3, lines 1-6), determining an address mode based on said bit (column 3, lines 10-12); comparing contents of a first register to contents of a second register if the bit is in a first state (column 3, lines 1-6);

or comparing the contents of the first register to contents of a non-register location if the bit is in a second state (column 3, lines 1-12), and skipping a subsequent instruction based on results of the comparison (column 1, lines 12-16).

As per claim 13:

Kreitzer teaches a system, comprising: a main processor unit (Fig 1); and a co-processor (Fig 1 # 2) coupled to said main processor unit, wherein said co-processor executes a test and skip instruction that includes a first register reference and a second register reference (Figures 1 # 4, column 2, lines 13-17) and causes the processor to compare the register value stored in a register corresponding to the first register reference and a second value associated with the second register reference (column 1, lines 49-55) and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison (column 1, lines 55-61).

As per claim 22:

Kreitzer teaches a programmable logic device comprising; control logic (Fig 1 # 1, column 2, lines 14-15) and a means for executing a test and skip instruction that includes a first register reference identifying a first register having a register value and a second register reference identifying a second register also having a register value (Figures 1 # 4, column 2, lines 13-17); for comparing the register value stored in the first register and a second value associated with the second register reference (column 1, lines 49-55), and for executing or not executing a subsequent instruction that follows the test and skip instruction based on the comparison (column 1, lines 55-61).

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 4,003,033 A, US Pat no. 4,028,668 A, and US Pat no. 4,038,537 A mention the same system of testing using an ALU and registers are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui

Art Unit 2138
12/05/2005